

Abstract

A content addressable memory (CAM) architecture. In one embodiment, the CAM architecture includes a CAM array including a plurality of rows of CAM cells to compare, in a first compare operation, comparand data with data stored in the rows and output match results on a plurality of match signal lines; a timed storage circuit having data inputs coupled to the match signal lines and an enable input; and a dynamic timing generator circuit including a first compare circuit to perform a second compare operation to generate an enable signal coupled to the enable input to enable the timed storage circuit to capture the match results.